5 TPC/MCH readout ASIC - SAMPA

Operating the TPC at a PbPb collision rate of 50 kHz requires the present limitations imposed by the operation of the gating grid to be overcome. Thus, the present MWPC based readout chambers will be replaced by GEM detectors, which feature intrinsic ion blocking without additional gating and exhibit excellent rate capabilities. As the drift time will be higher than the average time between interactions a trigger-less, continuous readout is implemented. This implies the upgrade of the existing front-end ASICs to a new readout ASIC, the SAMPA ASIC, providing continuous readout.

Furthermore, in order to operate the muon chambers (MCH) with an interaction rate of 50 kHz the present front-end electronics cannot be used and will be replaced by the SAMPA ASIC. The SAMPA ASIC adapts to different detector signals with programmable parameters.

The SAMPA ASIC is an evolution of the presently used TPC front-end electronics, where front-end amplifier and shapers sit in the 16-channel PASA ASIC [7][25]. The 16-channel ALTRO [26] chip digitizes, processes, compresses and stores the data in a multi-event memory. The Analog-to-Digital converters embedded in the chip have a 10-bit dynamic range and are used in the TPC at 10 MHz. After digitisation, a pipelined Data Processor is able to remove from the input signal a wide range of perturbations, related to the non-ideal behaviour of the detector, temperature variation of the electronics and environmental noise. Moreover, the Data Processor is able to suppress the pulse tail within 1 μs after the peak with 1 % accuracy, in order to improve their identification. The signal is then compressed by removing all data below a programmable threshold, except for a specified number of pre- and post-samples around each peak. This produces non-zero data packets. Eventually, each data packet is marked with its time stamp and size - so that the original data can be reconstructed afterwards - and stored in the multi-event memory. A further evolution of the system is the S-ALTRO ASIC [27]. The architecture is based on the ALTRO ASIC. The main difference is the integration of the charge shaping amplifier in the same IC. The SAMPA ASIC will integrate 32 channels of the full data processing chain and support continuous and triggered readout. The design of the SAMPA has already been started, taking the additional specifications compared to its predecessors into account.

5.1 System overview

SAMPA contains positive/negative polarity Charge Sensitive Amplifiers (CSA), which transform the charge signal into a differential semi-Gaussian voltage signal, that is digitized by a 10-bit 10 Msamples/s ADC. After the ADC a digital signal processor eliminates signal perturbations, distortion of the pulse shape, offset and signal variation due to temperature variations. SAMPA contains 32 channels per chip that concurrently digitize and process the input signals as shown in Fig. 5.1. The data readout takes place continuously at a speed of up to 1.28 Gbps by four 320 Mb/s e-links [12].

The data readout can be performed in continuous mode or triggered mode. In continuous mode the readout of a programmable number of samples is performed trigger-less if the input

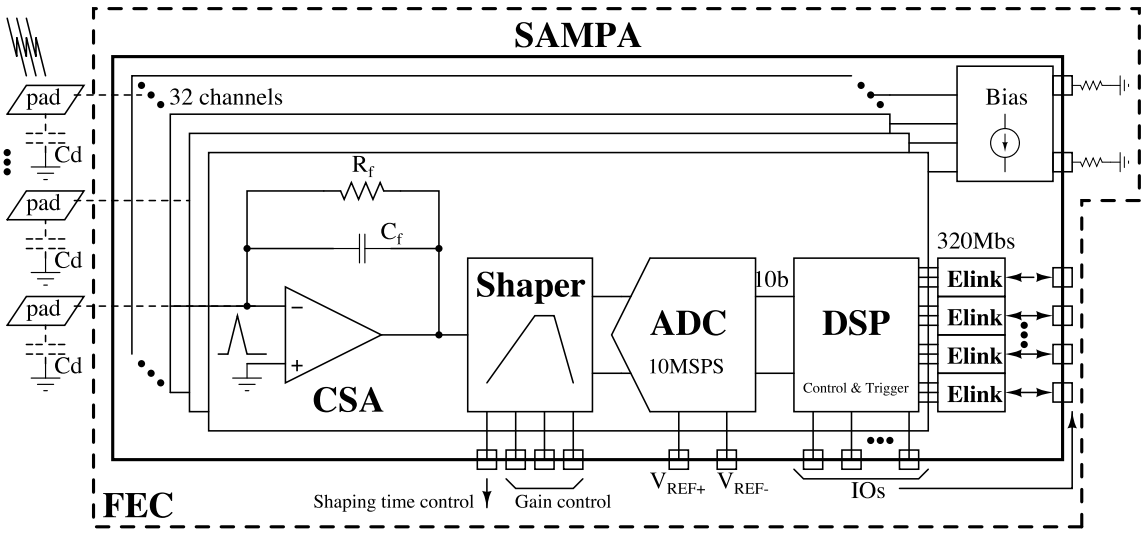

Figure 5.1: System block diagram

signal exceeds the programmable threshold value. For the TPC application a design rate of 50 kHz with 30 % occupancy is assumed. For the MCH the design rate is 100 kHz and 10 % occupancy. Software triggers are accepted during readout in continuous mode for calibration and synchronisation purposes. In triggered mode data readout of programmable number of samples is performed only upon reception of an external trigger with a maximum latency < 9.6 μs. Optionally all channels can be read out, not only those crossing the threshold. Triggers arriving during an active readout will be accepted. In that case the active readout will be extended by the new arriving trigger for the programmable number of samples and status information is sent to acknowledge the readout extension. Optionally a programmable number of pre/post samples before/after the input signal crossed the threshold in continuous mode or the external trigger mode arrived can be read out.

5.2 ASIC building blocks

The SAMPA ASIC is composed of a positive/negative polarity Charge Sensitive Amplifier (CSA) with a capacitive feedback C_f and a resistive feedback R_f connected in parallel, a Pole-Zero Cancellation (PZC) network, a high pass filter, two bridged-T second order low pass filters, a non-inverting stage, a 10 Msamples/s 10-bit ADC and a Digital Signal Processor(DSP) block, as shown in Fig. 5.2. Optionally the ADC can operate at 20 Msamples/s. The first shaper is a scaled-down version of the CSA and generates the first two poles and one zero. A copy of the first shaper connected in unity gain configuration is implemented in order to provide a differential mode input to the next stage. The second stage of the shaper is a fully differential second order bridged-T filter and it includes a Common-Mode Feed-Back network (CMFB). The non-inverting stage adapts the DC voltage level of the shaper output to use the full dynamic range of the ADC. It consists of a parallel connection of two equally designed Miller compensated amplifiers. The ADC is a differential 10-bit 10 Msamples/s SAR (successive approximation) ADC implemented with a low power switching technique. The DSP part is composed of digital filters, a data format unit, a ring buffer, a trigger manager block, a configuration register bank, a control state machine, and four 320 Mb/s e-links. The chip will be fabricated in 0.13 μm CMOS technology.

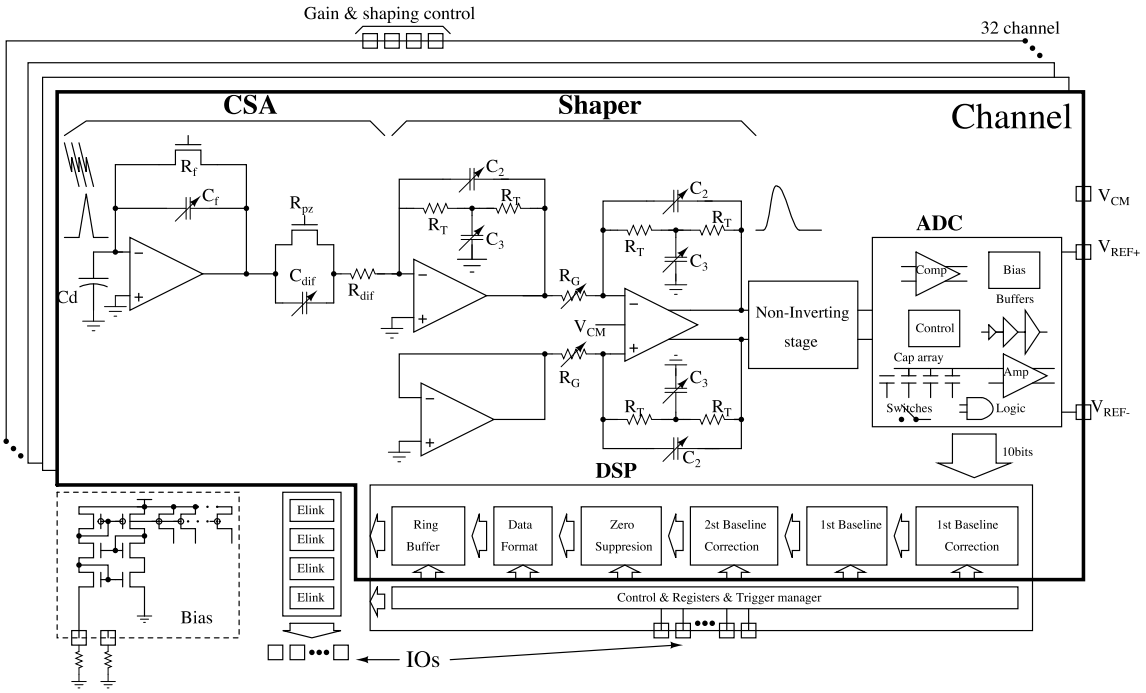

Figure 5.2: Block diagram of the SAMPA ASIC.

5.2.1 Front-end

Since the charge (Q_i) delivered by the TPC or MCH detectors is very small and short (typically 7 μA during 1 ns), it is unsuitable for immediate signal processing. Therefore, the input signal is first integrated and amplified by the CSA producing at its output a voltage signal (V_{CSA}), whose amplitude is proportional to the total charge Q_i and characterized by a long decay time constant $\tau = R_f \cdot C_f$. The C_f values are 600 fF@ts=80 ns , 1.2 pF@ts=160 ns and 2.4 pF@ts=300 ns, that are defined by the gain and linear range requirement and the R_f value of $6M\Omega$ is defined by the noise specification [25][28]. The relatively long discharge time constant of the CSA (τ) makes it vulnerable to pile-up. The low frequency part of the pulse is then removed by the high pass filter ($C_{dif} \cdot R_{dif}$). Due to the exponential decay of the CSA feedback network in combination with the differentiator network (R_{dif}, C_{dif}), an undershoot is created at the shaper output with the same time constant as the CSA of $\tau = R_f \cdot C_f$. This undershoot is removed by creating a pole-zero cancellation circuit by adding a resistance R_{pz} in parallel to the capacitor C_{dif} in the differentiator stage. It creates a Zero in the transfer function that cancels the low frequency pole introduced by the CSA feedback network [29][30]. The chosen topology of the CSA amplifier (Fig. 5.3) is based on a single-ended folded cascode amplifier followed by a source follower. The CSA has been optimized for the specification of detector capacitance and shaping time listed in Tab. 5.1.

The CSA shaping time can be configured to values of 80 ns and 160 ns for the TPC and 300 ns for the MCH. The sensitivity can be set to 20 or 30 mV/fC for the TPC and 4 mV/fC for the MCH by two external pins. As shown in Fig. 5.3, switches S_1-S_2 are used to adjust capacitances C_f and S_3 - S_4 to adjust C_{dif} for each case of peaking time. The capacitors of the T-bridge network of the semi-Gaussian shaper are adjusted for 80 ns, 160 ns or 300 ns of shaping time achieved by placing additional capacitors in parallel. It is performed with switches based on NMOS and PMOS transistors, sized to provide low series resistance. The required sensitivity is controlled by R_G trimming (Fig. 5.2) which is made by putting additional resistances in parallel.

Specification	**TPC**	**MCH**
Voltage supply	1.25V	1.25V
Polarity	Positive/Negative	Positive/Negative
Detector capacitance (Cd)	18.5pF	40pF - 80pF
Peaking time (ts)	80ns or 160ns	300ns
Shaping order	4th	4th
Equivalent Noise Charge (ENC)	< 536e@ts=80ns* or < 482e@ts=160ns*	< 950e @ Cd=40p* < 1600e @ Cd=80p*
Linear Range	100fC or 67fC	500fC
Sensitivity	20mV/fC or 30mV/fC	4mV/fC
Return to baseline time	<164ns@ts=80ns or <288ns@ts=160ns	<541ns
Non-Linearity (CSA + Shaper)	< 1%	< 1%
Crosstalk	< 0.3%@ts=80ns or < 0.2%@ts=160ns	< 0.2%@ts=300ns
ADC effective input range	2Vpp	2Vpp
ADC resolution	10-bit	10-bit
Sampling Frequency	10Msamples/s or 20Msamples/s	10Msamples/s
INL (ADC)	<0.65 LSB	<0.65 LSB
DNL (ADC)	<0.6 LSB	<0.6 LSB
SFDR (ADC)**	68dBc	68dBc
SINAD (ADC)**	57dB	57dB
ENOB (ADC)	9.2-bit	9.2-bit
Power consumption (per channel)		
ADC	2mW (4mW)	2mW (4mW)
CSA + Shaper	6mW	6mW
Channels per chip	32	32

*$R_{esd} = 70\Omega$
** @ 0.5MHz, 10Msamples/s

Table 5.1: Specifications of the new front-end ASIC (SAMPA).

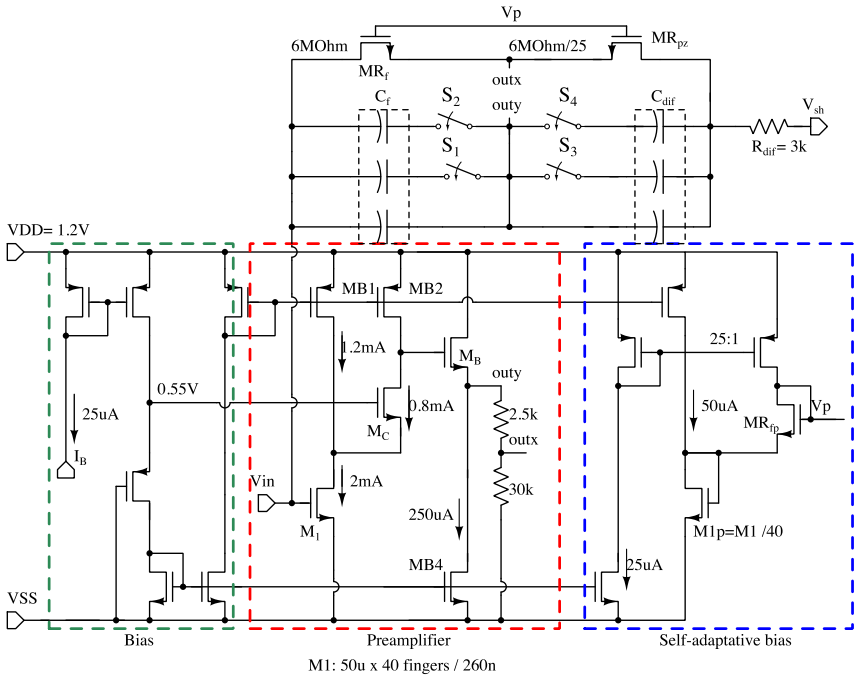

Figure 5.3: Transistor level schematic of the CSA.

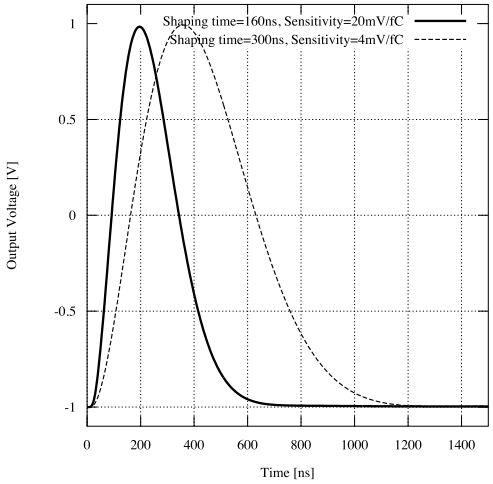

Figure 5.4: Output pulse waveform of the semi-Gaussian shaper.

The maximum amplitude of the output pulse is 2 Vpp. The output pulse waveform of the semi-Gaussian shaper is shown in Fig. 5.4 for 160 ns of shaping time (20 mV/fC of sensitivity) and 300 ns of shaping time (4 mV/fC of sensitivity).

The CMFB network of the second shaper stage establishes a stable common-mode voltage V_{CM} of 600 mV at the output of the second shaper. The chosen CMFB network consists of a resistor-capacitor network. This configuration takes the average of the two amplifier outputs and compares it with an externally given voltage V_{CM} and adjust the polarization current of the first stage of the amplifier.

A capacitive successive approximation (SAR) topology is used to design the 10Msamples/s 10-bit full differential ADC. The block diagram of the ADC is shown in Fig. 5.5. The main parts of

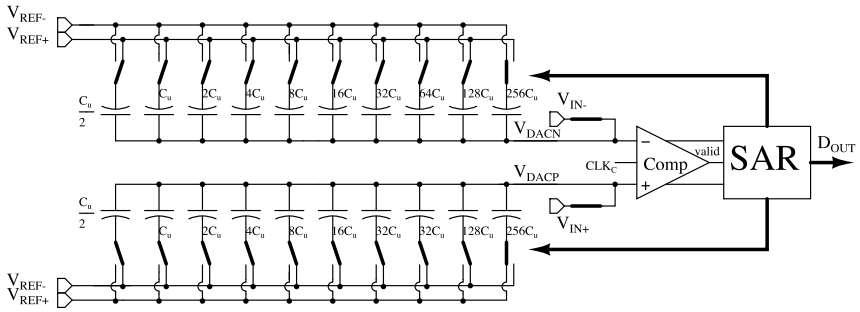

Figure 5.5: The block diagram of the 10b SAR ADC

the circuit are: capacitive array, switches, comparator and the SAR control logic. The capacitor array performs sample and hold and the digital to analog converter functions. A switching strategy with low energy dissipation per cycle is utilized.

The chip will be fabricated in TSMC 0.13 μm CMOS technology with nominal voltage supply of 1.2 V. The analog blocks and digital blocks will have separate supply pads (Voltage supply and ground) with high isolation to avoid digital noise coupling. A 25 μA stable current is generated on chip to bias the CSA and the Semi-Gaussian shaper (32 channels). An external resistor of high precision is used to control the bias current value. Another external resistance is used to control the bias of the ADC. It minimizes switching noise coupling from the ADC.

5.2.2 Digital signal processing

The signal processing is performed in 4 steps: a first correction and subtraction of the signal baseline, the cancellation of long-term components of the signal tail, a second baseline correction and zero suppression.

The first baseline correction (BC1) purpose is to decrease noise and systematic error effects. This block has two operation modes: subtraction mode and conversion mode. The subtraction mode consists of subtracting a value from the input (D_{in}). This mode is divided in three kinds:

- Fixed: subtracts a constant value, called fixed pedestal, set previously in a register.
- Time dependent: subtracts a variable value which is stored in the pedestal memory (4096x10-bit). The values are accessed from first to last, so the order of the subtractions is the same for every processing window.
- Self-calibrated: a baseline value is calculated outside the processing window. It is called variable pedestal (V_{pd}), and its calculation is performed by an infinite impulse response (IIR) filter. If this option is selected, the filter is activated receiving as input D_{in} and providing $D_{in} - V_{pd}$ as output, so V_{pd} is not accessible.

The conversion mode uses the input data to address the pedestal memory, so we have the output as a function of V_{in}.

The Tail Cancellation Filter (TCFU), is a 4-stage IIR filter used with the intention of cancelling a slowly varying signal. The signal rise time is fast, but its fall time is much slower and has a rather complex shape that varies from pad to pad.

The second level of baseline correction (BC2) is applied to the signal during the PTW (Processing Time Window) and corrects signal perturbations created by non-systematic effects. The

threshold values have a constant component which is the same for the whole chip and a variable component which is channel specific so it must be set individually for each of the channels.

The zero suppression (ZSU) block eliminates data below a programmable threshold. An option to switch off the zero suppression is foreseen.

5.3 Configuration and control

The SAMPA ASIC is configured via an independent serial interface. Data readout can take place at the same time. In order to keep compatibility with the GBT slow control adapter ASIC, SCA [17], SAMPA can be configured via an I2C interface. In addition, a high speed serial configuration and control interface operating at 320 Mb/s serial interface using one input and one output differential pair, is foreseen.

5.4 Trigger and dead time

SAMPA supports two trigger modes: external and continuous mode. The readout works identically in both trigger modes. The number of samples per event is programmable (0 to 4095), as well as the number of pre-samples (0 to 63), which is the number of samples acquired before the external trigger arrived or the signal went above threshold. Also the number of post samples after the signal went below threshold is programmable (0 to 7). The number of samples per event and number of pre-samples are common to the 32 channels.

The trigger is sent either via an external pin or via an instruction with maximum latency $<= 9.6$ μs. In continuous mode the ASIC operates without an external trigger. It reads-out a channel when the data rises above a threshold in this channel and optionally reads-out the whole chip.

Provided the average interaction rate and occupancy does not exceed specifications the SAMPA cannot get busy as it is specified for continuous readout. During operation the interaction rate or occupancy might get too high for the design readout rate. In that case the SAMPA data buffers will overflow. The SAMPA readout controller will truncate the readout packets, balance the readout buffers and inform the DAQ in the data header that truncation occurred. In triggered operation a trigger could be issued during an active readout. In that case the reception of this trigger is acknowledged by sending a packet trailer and the data readout is extended by the number of programmable samples. Provided the interaction rate does not exceed specifications no data loss occurs. This feature also allows accommodation of the periodic heartbeat trigger in both triggered mode and continuous mode. After a heartbeat trigger the SAMPA needs to respond immediately with a header/trailer and optional status information. Optionally the data readout before the heartbeat trigger is continued or stopped. In any case there is no need to send a fast busy signal to the TPC. Too many triggers are indicated in the trailers. Too much data (too high occupancy or interaction rate) will fill the buffers and automatic truncation is communicated to the DAQ. Under nominal operation conditions the SAMPA will not get busy. However, in order to cope with unforeseen states where the SAMPA gets blocked, the CRU forwards status information to the CTP which throttles or stops the triggers. This transmission scheme is slower than a dedicated busy link from the front-end to the TPC but completely sufficient for this purpose.

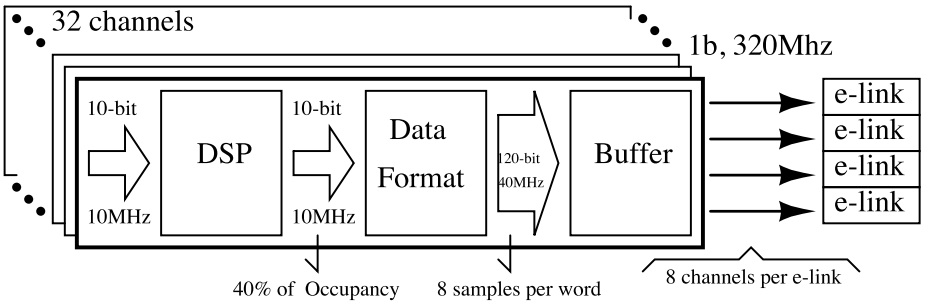

Figure 5.6: Data block diagram

5.5 Readout

In continuous mode, once data are acquired they are formatted and stored in a FIFO, where they wait to be sent to the 320 Mb/s serial e-links, which send them off the chip. There are 32 channels and 4 e-links of 320 Mbit/s. Each e-link is connected to 8 channels transmitting either non-DC balanced or 8b10b encoded data stream. The readout controller polls the data FIFOs and reads them out in a round robin based fashion. The size of the data FIFOs still needs to be defined. It shall be done as a trade-off between chip area and probability of truncated events on high occupancy periods.

The TPC application defines the maximum data band width. It is designed for a channel occupancy of 30 % and a sampling rate of 10 MHz. Given the 32 channels * a sampling rate of 10 MHz * a word length of 10 bit * 30 % occupancy, a data rate of 960 Mb/s per ASIC or 240 Mb/s per e-link needs to be accommodated. The 320 Mb/s e-links offer sufficient margin for transmission overhead. For pedestal runs, where the zero suppression is deactivated the readout is stopped when the buffers are full and restarted once they have been read out.

SAMPA operates with frame based readout. Once the readout starts, the header containing the bunch crossing counter, trigger origin and number of samples per event is sent. When the readout finishes a trailer containing the total number of 10-bit words on that event, data truncated and status information is sent. Also, a header-trailer pair is sent in order to tell the back-end electronics whenever the internal time stamping counter overflows and starts from zero.

When the SAMPA is operated together with the GBTx ASIC it receives a 40 MHz clock from the GBT. This clock signal is used to align the SAMPA word boundaries to the transmission phase of the GBTx. In order to adapt the number of e-link outputs to application data rate, the hit data can be routed through either all 4, 2 or 1 e-link, programmable via instruction. Furthermore data from neighbouring ASICs can be routed to the ASIC output (daisy chained readout) to further decrease number of output links in system. An additional e-link input is available for this purpose. In the MCH application this allows daisy chaining two SAMPA ASICs and the readout of one front-end card by one single e-link only. For test purposes of the detector system and the online computing system SAMPA allows to send pre-programmable data sequences. The SAMPA data flow block diagram is shown in Fig. 5.6.

5.6 ASIC I/Os

All the digital IO of the SAMPA ASIC are differential SLVS ports. The following list describes the SAMPA periphery:

Digital inputs:

- Digital clock: 320 MHz, a jitter of less than 30 ps RMS is expected.
- ADC reference clock: 10 MHz, optionally it can be produced from the digital clock. The phase of the ADC reference clock can be adapted to the GBT alignment clock.
- GBT alignment clock: 40 MHz, this signal allows alignment to the GBT transmission word phase.
- Reset global: resets all registers.
- Sync: This signal resets internal event counter and time stamp.
- Trigger: external trigger signal, synchronised to internal 40 MHz with programmable phase.
- e-link data input: allows merging data stream of neighboring ASIC.
- Address: 5 bit hard-coded address field which can be read via the configuration ports.
- High speed serial instruction input (8b10).
- Sensitivity control (gc0 and gc1): 2 pin (This value also can be programmed)
- Shaping time control (ptc0 and ptc1): 2 pin (This value also can be programmed)

Digital outputs:

- 4 e-link outputs: 320 Mbit/s data stream, programmable non-DC balanced or 8b10.
- Readout active signal:
- Full signal: is active, when buffers in the ASIC are full, data loss occurs and data readout is truncated.
- High speed serial instruction output (8b10).

Digital Input/Outputs:

- I2C interface.

Analog inputs:

- 32 Detector inputs: 32 pins
- External bias resistances: 2 pins
- Reference voltages (V_{REF-}, V_{REF+}): 2 pins
- Common voltage (V_{CM}): 1 pin

The sensitivity and shaping time programming options of the ASIC are listed in Tab. 5.2.

ptc0	ptc1	gc0	gc1	Shaping time	Sensitivity
0	0	0	0	160ns	30mV/fC
0	0	1	0	160ns	20mV/fC
0	0	0	0	80ns	30mV/fC
0	0	1	1	80ns	20mV/fC
1	1	1	1	300ns	4mV/fC

Table 5.2: Gain an shaping time programming options of the ASIC.

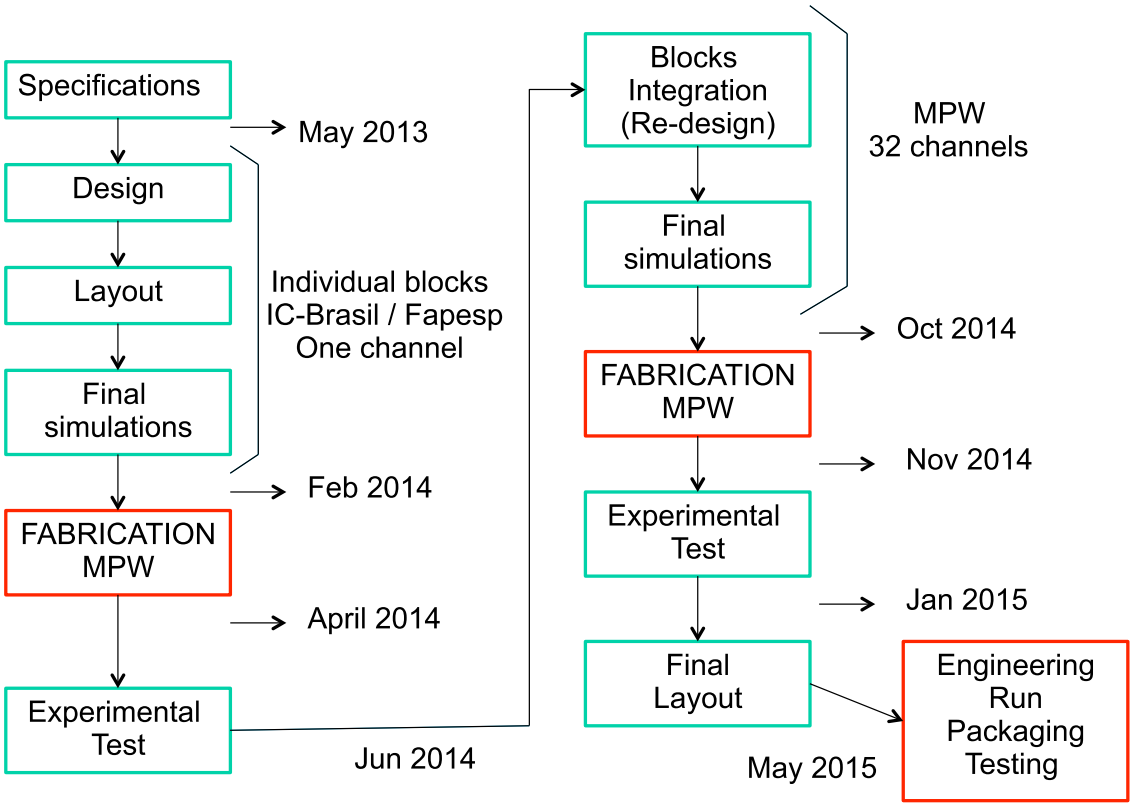

Figure 5.7: Schedule of the TPC/MCH readout ASIC project

5.7 Schedule, funding and institutes

The project schedule is presented in Fig. 5.7. Presently the project is in the design phase. The analog blocks are ready to start the layout phase.

Two prototyping runs (MPW: Multi-Project Wafer) will be performed:

1. The first run planned for November of 2013 will contain each block separately and a complete version of one channel (Preamplifier, Shaper, ADC and digital blocks). The test boards will be designed and implemented by Polytechnic School of the University of Sao Paulo or by the ALICE collaboration. The radiation tolerance test will be performance at Nuclear Physics Department of USP. More detailed tests will be conducted by the TPC and MCH Team.

2. The second run is planned for August 2014, which will contain the 32 channels, all integrated on one die. The purpose is to test the whole system, among them: power consump-

item	cost
MPW	2 * 50 kUSD
Full scale submission	2 * 400 kUSD
Wafer production	875 kUSD
Total	1775 kUSD
Number of MCH + TPC SAMPA	52000
Price per ASIC out of 52000	34 USD
Packaging & testing per ASIC	10 USD
Price per packaged and tested ASIC incl. 10 % spares	44 USD
Price per packaged and tested ASIC incl. 10 % spares	40 CHF

Table 5.3: SAMPA cost estimate.

tion, the noise and crosstalk performance.

The final chip is being planned to be produced in May of 2015.

In Tab. 5.3 SAMPA cost estimate is made. The estimate assumes prices for a similar technology, as TSMC prices available via the CERN frame contract are not yet available. The cost estimate is based on 2 multi project engineering runs (MPW), 2 full scale submissions, a final ASIC size of 65 mm^2 and an ASIC yield of 60 %. Using these numbers this estimate refers to a upper price limit. On one wafer a silicon area of 25200 mm^2 (60 reticles x 21 mm x 20 mm) is assumed, corresponding to 387 ASICs per wafer and, applying the yield, 232 working ASICs per wafer. In total 52000 ASICs are needed (without spares) and thus 224 wafers or 250 wafers with spares included are required. Assuming 3500 USD per wafer the production cost is 875 kUSD.

The project has the following funding sources:

1. Special program for integrated circuits fabrication of Brazilian public universities
2. Regular project submitted to FAPESP for chip development
3. FAPESP project to be submitted for the engineering fabrication run

Other funding agencies include

- Ministry of Science, Technology and Innovation
- University of Sao Paulo
- CNPq agency: National Counsel of Technological and Scientific Development

Table 5.4 shows the involved institutes.

Institutes
EPUSP, Escola Politécnica, Universitade de São Paulo, Brazil
IFUSP, Instituto de Fisica, Universidade de São Paulo, Brazil
University of Bergen, Norway
IPNO, Institut de Physique Nuclaire d'Orsay, Université de Paris-Sud, IN2P3/CNRS, France
SPhN, Service de Physique Nuclaire, CEA-IRFU Saclay, France

Table 5.4: SAMPA institutes.